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(71) Applicant: **SAMSUNG SEMICONDUCTOR, INC.**
**3725 North First Street**
**San Jose, California 95134(US)**

(72) Inventor: **Chang, Shuen-Chin**
**7227 Sleepy Creek Drive**
**San Jose, California 95120(US)**

(74) Representative: **Jones, Ian et al**
**POLLAK MERCER & TENCH High Holborn**
**House 52-54 High Holborn**
**London WC1V 6RY(GB)**

## (54) Voltage level translation circuit.

(57) The invention provides a static inverter-type TTL/CMOS level translator including transistors (Q2 & Q5) to suppress hot electron effects. The transistors limit maximum VDS to VCC-VTN at the first and second gain stages. Resistors (R1 & R2) serve as a virtual VCC modulator to minimize voltage variations, stabilizing the VIL/VIH trip point. The resistors (R1 & R2) also minimize standby current so that the translator can be used in a low standby current environment. The translator provides faster speed, wider process margins, better reliability and lower standby current than prior art translators.

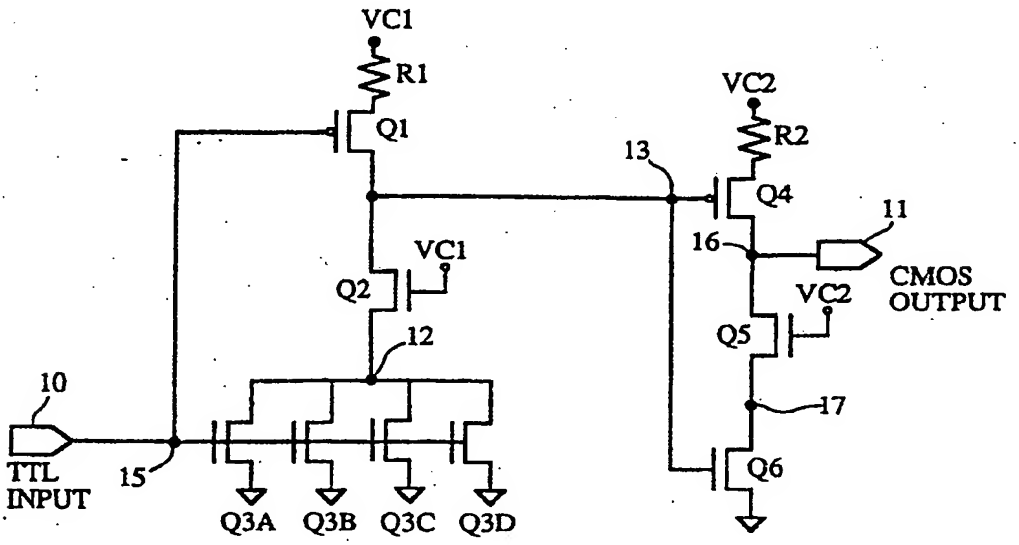


FIGURE 2

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are described in order to provide a more thorough description of the present invention. It will be apparent, however, to one skilled in the art, that the present invention may be practiced without these specific details. In other instances, well known features have not been described in detail so as not to obscure the present invention.

An example of a prior art static inverter type of TTL/CMOS level translator is illustrated in Figure 1. The TTL input 10 is coupled at node 15 to the gates of transistor Q1 and transistor string Q3A-Q3D. Transistor Q1 is a P-type transistor whose source is coupled to voltage VC1. The drain of transistor Q1 is coupled to the drains of transistors Q3A-Q3D at node 12 and to the gates of transistors Q4 and Q6. The sources of transistors of Q3A-Q3D are coupled to ground. Transistors Q3A-Q3D are N-type transistors. The source of P-type transistor Q4 is coupled to voltage VC2. The drain of transistor Q4 is coupled to the drain of N-type transistor Q6 at node 14. The source of transistor Q6 is coupled to ground. The CMOS output 11 is taken from node 14.

The static inverter translator of Figure 1 consists of two inverter stages. The first inverter stage is comprised of P channel Transistor Q1 and N channel transistors Q3A-Q3D. The output of this first stage at node 12 is coupled to the second inverter stage. The second inverter stage is comprised of P type transistor Q4 and N type transistor Q6.

For a particular input voltage VIL from the TTL circuit, the translator should output a logical "0". For an input VIH voltage from the TTL circuit, the translator circuit should be a logical "1". However, the TTL input conditions are not always stable. In addition, hot electron effects can degrade VTN. Therefore, the VIL/VIH trip point may vary.

When the input 10 is low, (e.g., less than 0.8 volt) transistor Q1 is turned on and transistors Q3A-Q3D are off. The output of the first inverter stage at Node 12 is VC1. This voltage turns transistor Q4 off and turns transistor Q6 on. This drops the signal at the output of the second inverter stage at Node 14 low, providing a logical "0" output. When the input 10 is high, transistors Q3A-Q3D are turned on. Thus, the output at Node 12 is low (e.g., 0.8 volt). This turns on transistor Q4 and turns transistor Q6 off, so that the output at Node 14 of the second inverter stage is high approaching VC2, providing a logical "1" output 11.

Due to hot electron effects, the voltage VTN can suffer from degradation at transistors Q3A-Q3D. This can lead to incorrect output from the TTL/CMOS level translator.

The hot electron effect degrades VT for transistors Q3A-Q3D. The voltage at node 12 is made unstable by this effect. When the input 10 switches from VIL to VIH, the node 12 is to be discharged through transistors Q3A-Q3D. However, hot electron effects can shift VT higher for transistors Q3A-Q3D. If VT is shifted higher than designed specifications, node 12 may not discharge at the predicted VIL/VIH trip point. This can lead to a false low reading at the output of the translator.

The prior art translator of Figure 1 also suffers in low standby current conditions. Because, for example, when input 10 is at VIH (e.g., 2.4 volts), both Q1 and Q3A-Q3D are turned on at the same time. The standby current of the first inverter stage is mainly determined by the turn-on resistances of Q1 and Q3A-Q3D, and not current-limited for the low standby current applications. Also, because the P-channel transistor Q1 and N-channel transistor Q3A-Q3D are ratioed, a stable trip point depends on a stable power supply VCC. If the power supply varies from 4.5 to 5.5 volts, for example, a full 1 volt variation is seen by transistor Q1. Consequently the VIL/VIH trip point varies. The present invention provides a virtual VCC which is less sensitive to power supply fluctuations.

The present invention also utilizes two inverter stages to accomplish TTL/CMOS level translation. The first stage (input stage) is comprised of a complementary pair of transistors, one P type and one N type. The transistor pair is gate coupled to the TTL input voltage. A third transistor is coupled between the drains of the complementary pair and gate coupled to a supply voltage. This extra transistor clamps the voltage at the drain of the N-channel transistors to a fixed maximum level so as to suppress hot electron effects.

The output of the first inverter stage is coupled to the gates of a second complementary pair of transistors. As in the first stage, an additional transistor is coupled between the drains of the complementary pair to suppress hot electron effects. This additional transistor is gate coupled to a second supply voltage which may be identical to the first supply voltage.

Resistors are used between the sources of the P channel transistors and the supply voltages to provide a virtual VCC at the source of the P channel transistors. The resistors reduce the effects of voltage swings in the supply voltages VC1 and VC2, so that the net effect on the virtual supply voltage is minimized. This stabilizes the VIL-VIH trip point.

The preferred embodiment of the present invention is illustrated in Figure 2. The present invention also comprises a static inverter type of TTL/CMOS translator. The present invention provides resistors R1 and R2 to minimize the standby current of a prior art-type of level translator. Resistor R1 is coupled between voltage VC1 and the source of transistor Q1. Resistor R2 is coupled

6. A circuit as claimed in any preceding claim wherein the first conductivity type comprises P-type conductivity.

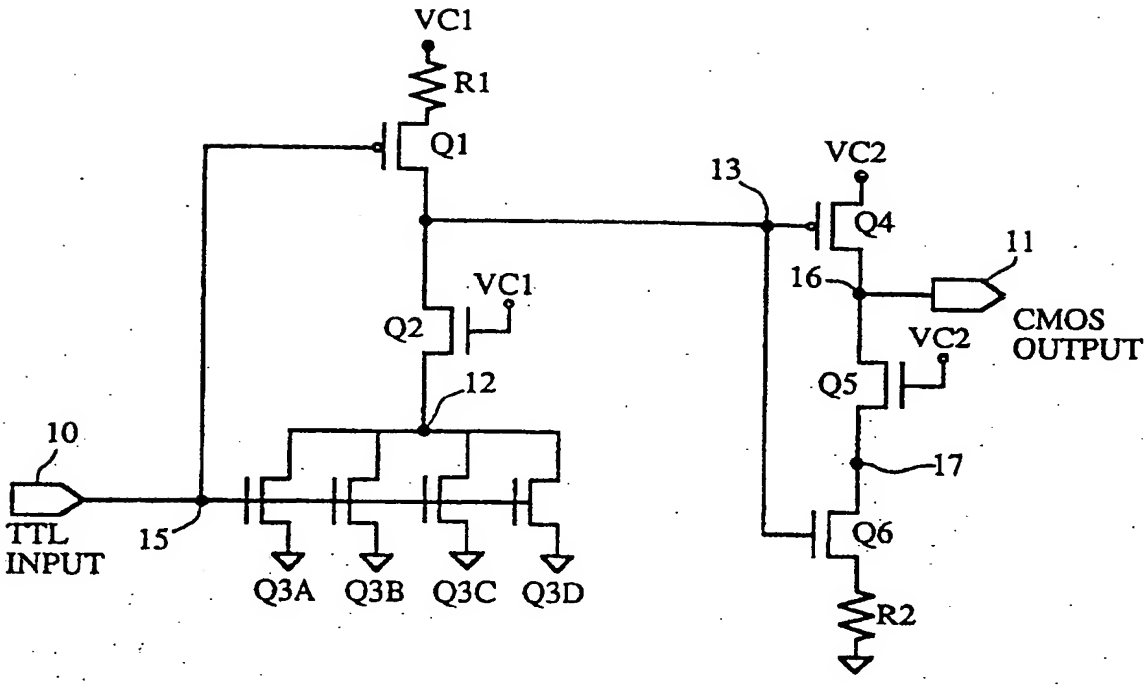


FIGURE 3